IN THE SPECIFICATION:

Replace the paragraphs at page 43, line 17 to page 44, line 3 with the following amended paragraphs:

In the latch (A) 303 after completing sending the digital video signals to the latch (B) 304, it is performed to write into the digital video signals in accordance with the timing signal from the shift ~~resister~~ register 302.

The gate signal driving circuit 305 has the shift ~~resister~~ register 306 and the buffer 307. According to circumstances, the level shift is provided.

In the gate signal driving circuit 305, the timing signal from the shift ~~resister~~ register 306 is inputted to the buffer 307, and then to a corresponding gate signal line. The gate electrodes of the first switching TFTs for one line of pixels are connected to the gate signal lines, and all of the first switching TFTs of the one line of pixels must be placed in an ON state simultaneously. A circuit, which is capable of handling the flow of a large electric current, is therefore used for the buffer.